CLB and Interconnect Matrix 205 CLB & Interconnect Switching Device Logic 103 Configuration Memory Cell 100 Latch 101 User Clock 204 Select Transistor Configuration Array 202 Configuration Array 203 Configuration Array 201 Configuration Data 105 ♠ Configuration Select 104

Figure 1 (Prior Art)

Figure 2

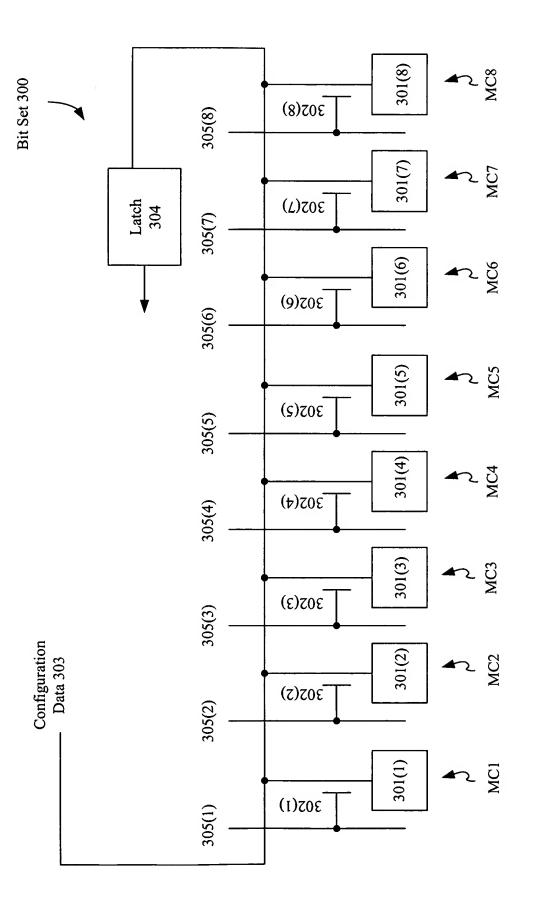


Figure 3

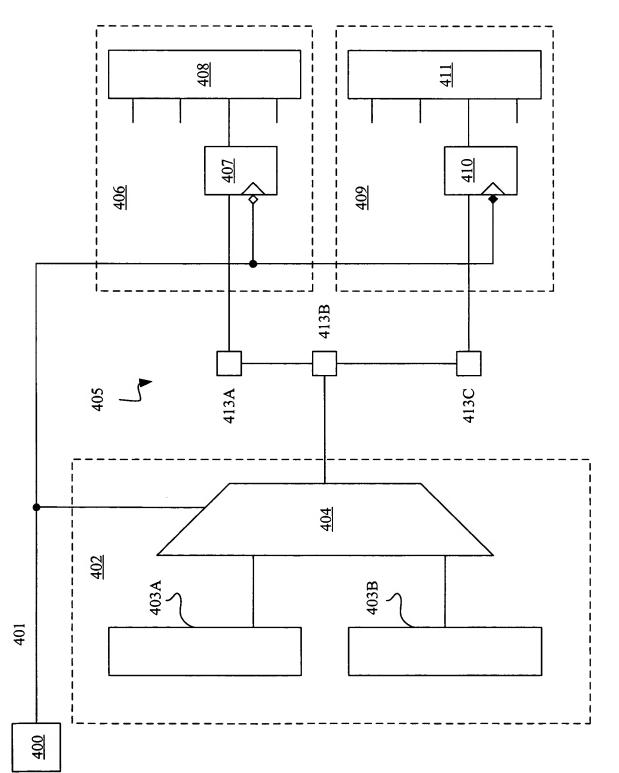


Figure 4A

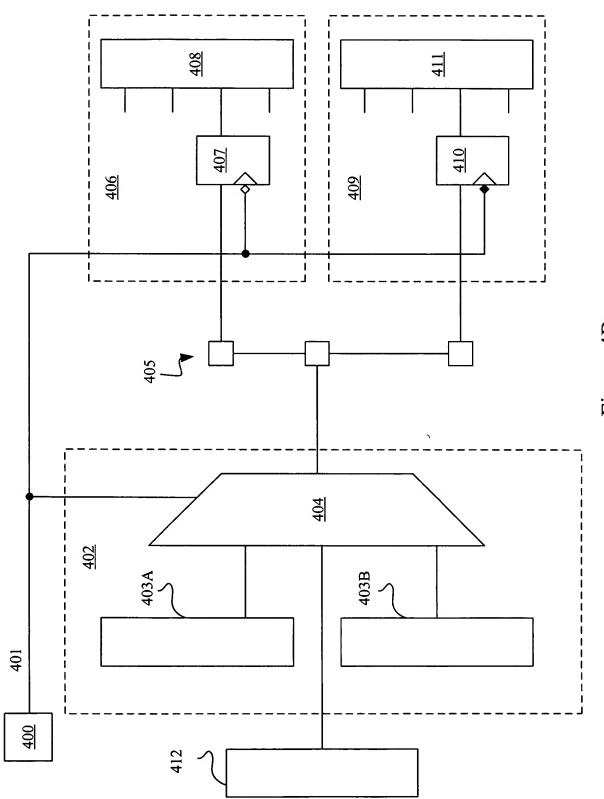


Figure 4B

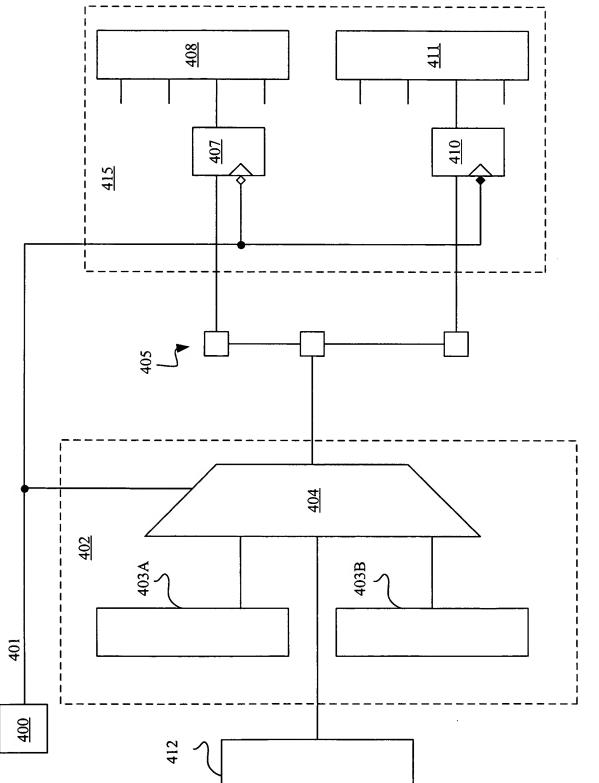


Figure 4C

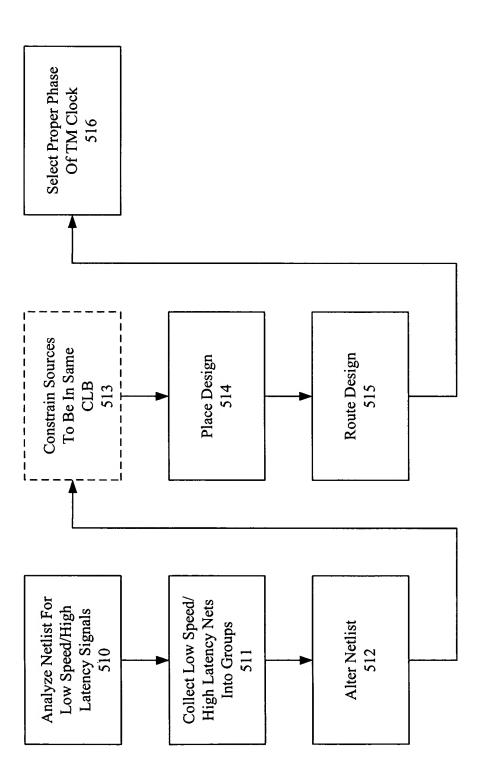


Figure 5A

